

This Page Is Inserted by IFW Operations  
and is not a part of the Official Record

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problem Mailbox.**

Japanese Patent Laid-Open Publication No. Heisei 9-8205

[TITLE OF THE INVENTION]

RESIN-ENCAPSULATED SEMICONDUCTOR DEVICE

5

[CLAIMS]

1. A resin-encapsulated semiconductor device using  
a lead frame which is shaped in accordance with a two-step  
etching process to a body wherein a thickness of inner  
10 leads is less than that of the lead frame blank,  
comprising:

inner leads having the thickness less than that of the  
lead frame blank; and

terminal columns integrally connected to the inner  
15 leads and having the same thickness with the lead frame  
blank, the terminal columns possessing a column-shaped  
configuration which is adapted to be electrically connected  
to an external circuit, the terminal columns being disposed  
outside of the inner leads in a manner such that they are  
20 coupled to the inner leads in a direction orthogonal to the  
thickness-wise direction thereof, the terminal columns  
having terminal portions arranged on top ends thereof, the  
terminal portions being made of solders, etc. and exposed  
to the outside beyond a resin encapsulate, each inner lead  
25 possessing a rectangular cross-section and having four

surfaces including a first surface, a second surface, a  
third surface and a fourth surface, the first surface being  
flushed with one surface of a remaining portion of the  
inner lead having the same thickness with the lead frame  
blank while being opposed to the second surface, and each  
5 of the third and fourth surfaces having a concave shape  
depressed toward the inside of the inner lead.

2. A resin-encapsulated semiconductor device using  
10 a lead frame which is shaped in accordance with a two-step  
etching process to a body wherein a thickness of inner  
leads is less than that of the lead frame blank,  
comprising:

15 inner leads having the thickness less than that of the  
lead frame blank; and

terminal columns integrally connected to the inner  
leads and having the same thickness with the lead frame  
blank, the terminal columns possessing a column-shaped  
configuration which is adapted to be electrically connected  
20 to an external circuit, the terminal columns being disposed  
outside of the inner leads in a manner such that they are  
coupled to the inner leads in a direction orthogonal to the  
thickness-wise direction thereof, portions of top ends of  
the terminal columns being exposed to the outside beyond a  
25 resin encapsulate, each inner lead possessing a rectangular

cross-section and having four surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

10           3.     The resin-encapsulated semiconductor device as claimed in claims 1 or 2, wherein a semiconductor chip is received inward of the inner leads, and electrodes of the semiconductor chip are electrically connected to the inner leads through wires, respectively.

15           4.     The resin-encapsulated semiconductor device as claimed in claim 3, wherein the lead frame has a die pad, and the semiconductor chip is mounted onto the die pad.

20           5.     The resin-encapsulated semiconductor device as claimed in claim 3, wherein the lead frame does not have a die pad, and the semiconductor chip is fastened to the inner leads using a reinforcing fastener tape.

25           6.     The resin-encapsulated semiconductor device as

claimed in claims 1 or 2, wherein the semiconductor chip is fastened by means of insulating adhesive to the second surfaces of the inner leads on one surface thereof on which the electrodes are located, and the electrodes of the semiconductor chip are electrically connected to the first surfaces of the inner leads through wires, respectively.

7. The resin-encapsulated semiconductor device as claimed in claims 1 or 2, wherein the semiconductor chip is fastened to the second surfaces of the inner leads by bumps thereby to be electrically connected to the inner leads.

[DETAILED DESCRIPTION OF THE INVENTION]

[FIELD OF THE INVENTION]

The present invention relates to a resin-encapsulated semiconductor device capable of meeting the requirement for an increase in the number of terminals and resolving problems which are caused in association with position shift and coplanarity of an outer lead.

[DESCRIPTION OF THE PRIOR ART]

FIG. 15(a) shows the configuration of a generally known resin-encapsulated semiconductor device (a plastic lead frame package). The shown resin-encapsulated semiconductor device includes a die pad 1511 having a

semiconductor chip 1520 mounted thereon, outer leads 1513  
to be electrically connected to the associated circuits,  
inner leads 1512 formed integrally with the outer leads  
1513, bonding wires 1530 for electrically connecting the  
5 tips of the inner leads 1512 to the bonding pad 1521 of the  
semiconductor chip 1520, and a resin 1540 encapsulating the  
semiconductor chip 1520 to protect the semiconductor chip  
1520 from external stresses and contaminants. This resin-  
encapsulated semiconductor device, after mounting the  
10 semiconductor chip 1520 on the bonding pad 1521, is  
manufactured by encapsulating the semiconductor chip 1520  
with the resin. In this resin-encapsulated semiconductor  
device, the number of the inner leads 1512 is equal to that  
of the bonding pads 1521 of the semiconductor chip 1520.  
15 And, FIG. 15(b) shows the configuration of a monolayer lead  
frame used as an assembly member of the resin-encapsulated  
semiconductor device shown in FIG. 15a. Such a lead frame  
includes the bonding pad 1511 for mounting the  
semiconductor chip, the inner leads 1512 to be electrically  
20 connected to the semiconductor chip, the outer lead 1513  
which is integral with the inner leads 1512 and is to be  
electrically connected to the associated circuits. This  
also includes dam bars 1514 serving as a dam when  
encapsulating the semiconductor chip with the resin, and a  
25 frame 1515 serving to support the entire lead frame 1510.

Such a lead frame is formed from a highly conductive metal such as a cobalt, 42 alloy (a 42% Ni-Fe alloy), copper-based alloy by a pressing working process or an etching process. FIG. 15(b)(D) is a cross-sectional view taken along the line F1-F2 of FIG. 15(b)(1).

Recently, there has been growing demand for the miniaturization and reduction in thickness of resin-encapsulated semiconductor device employing lead frames like the lead frame (plastic lead frame package) and the increase of the number of terminals of resin-encapsulated semiconductor package as electronic apparatuses are miniaturized progressively and the degree of the integration of semiconductor device increase progressively. Thus, recent resin-encapsulated semiconductor package, particularly quad plate package (QFPs) and thin quad flat packages (TQFPs) have each a greatly increased number of pins.

Lead frames having inner leads arranged at small pitches among lead frames for semiconductor packages are fabricated by a photolithographic etching process, while lead frames having inner leads arranged at comparatively large pitches among lead frames for semiconductor packages are fabricated by press working. However, lead frames having a large number of fine inner leads to be used for forming semiconductor packages having a large number of

pins are fabricated by subjecting a blank of a thickness on the order of 0.25 mm to an etching process, not a press working.

5 The etching process for forming a lead frame having fine inner leads will be described hereinafter with reference to FIG. 14. First, a copper alloy or 42 alloy thin sheet of a thickness on the order of 0.25 mm (a lead frame blank 1410) is cleaned perfectly (FIG. 14(a)). Then, a photoresist, such as a water-soluble casein photoresist  
10 containing potassium dichromate as a sensitive agent, is spread in photoresist films 1420 over the major surfaces of the thin film as shown in FIG. 14(b).

15 Then, the photoresist films are exposed, through a mask of a predetermined pattern, to light emitted by a high-pressure mercury lamp, and the thin sheet is immersed in a developer for development to form a patterned photoresist film 1430 as shown in FIG. 14(c). Then, the thin sheet is subjected, when need be, to a hardening process, a washing process and such, and then an etchant  
20 containing ferric chloride as a principal component is sprayed against the thin sheet 1410 to etch through portions of the thin sheet 1410 not coated with the patterned photoresist films 1420 so that inner leads of predetermined sizes and shapes are formed as shown in FIG.  
25 14(d).



Then, the patterned resist films are removed, the patterned thin sheet 1410 is washed to complete a lead frame having the inner leads of desired shapes as shown in FIG. 14(e). Predetermined areas of the lead frame thus  
5 formed by the etching process are silver-plated. After being washed and dried, an adhesive polyimide tape is stuck to the inner leads for fixation, predetermined tab bars are bent, when need be, and the die pad depressed. In the etching process, the etchant etches the thin sheet in both  
10 the direction of the thickness and directions perpendicular to the thickness, which limits the miniaturization of inner lead pitches of lead frames. Since the thin sheet is etched from both the major surfaces as shown in FIG. 14 during the etching process, it is said, when the lead frame  
15 has a line-and-space shape, that the smallest possible intervals between the lines are in the range of 50 to 100 $\mu$ m of the thickness of the thin sheet. From the viewpoint of forming the outer lead having a sufficient strength, generally, the thickness of the thin sheet must be about  
20 0.125 mm or above. Furthermore, the width of the inner leads must be in the range of 70 to 80  $\mu$ m for successful wire bonding. When the etching process as illustrated in FIG. 14 is employed in fabricating a lead frame, a thin sheet of a small thickness in the range of 0.125 to 0.15 mm  
25 is used and inner leads are formed by etching so that the

fine tips thereof are arranged at a pitch of about 0.1 mm.

However, recent miniature resin-encapsulated semiconductor package requires inner leads arranged  
5 pitches in the range of 0.13 to 0.15 mm, far smaller than 0.165 mm. When a lead frame is fabricated by processing a thin sheet of a reduced thickness, the strength of the outer leads of such a lead frame is not large enough to withstand external forces that may be applied thereto in the subsequent processes including an assembling process and a chip mounting process. Accordingly, there is a limit to the reduction of the thickness of the thin sheet to enable the fabrication of a minute lead frame having fine leads arranged at very small pitches by etching.

15 An etching method previously proposed to overcome such difficulties subjects a thin sheet to an etching process to form a lead frame after reducing the thickness of portions of the thin sheet corresponding to the inner leads of the lead frame by half etching or pressing to form  
20 the fine inner leads by etching without reducing the strength of the outer leads. However, problems arise in accuracy in the subsequent processes when the lead frame is formed by etching after reducing the thickness of the portions corresponding to the inner leads by pressing; for  
25 example, the smoothness of the surface of the plated areas

is unsatisfactory, the inner leads cannot be formed in a flatness and a dimensional accuracy required to clamp the lead frame accurately for bonding and molding, and a platemaking process must be repeated twice making the lead fabricating process intricate. It is also necessary to repeat a platemaking process twice when the thickness of the portions of the thin sheet corresponding to the inner leads is reduced by half etching before subjecting the thin sheet to an etching process for forming the lead frame, which also makes the lead frame fabricating process intricate. Thus, this previously proposed etching method has not yet been applied to practical lead frame fabricating processes.

(SUBJECT MATTERS TO BE SOLVED BY THE INVENTION)

On the other hand, because a pitch among inner leads is made narrow as the number of terminals is increased, it is considered important to know whether a problem is caused or not in association with position shift or coplanarity of an outer lead when implementing a chip mounting process. Accordingly, the present invention has been made in an effort to solve the problems occurring in the related art, and an object of the present invention is to provide a resin-encapsulated semiconductor device capable of meeting the requirement for an increase in the number of terminals

and resolving problems which are caused in association with position shift and coplanarity of an outer lead.

(MEANS FOR SOLVING THE SUBJECT MATTERS)

5           According to one aspect of the present invention, there is provided a resin-encapsulated semiconductor device using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of inner leads is less than that of the lead frame blank comprising: inner leads having the thickness less than that of the lead frame blank; and terminal columns electrically connected to the inner leads and having the same thickness as with the lead frame blank, the terminal columns positioned in a column-shaped configuration which is adapted to be electrically connected to an external circuit, the terminal columns being disposed outside of the inner leads in a manner such that they are coupled to the inner leads in a direction orthogonal to the thickness-wise direction thereof, the terminal columns having terminal portions arranged on top ends thereof, the terminal portions being made of solders, etc. and exposed to the outside beyond the resin encapsulate, outer surfaces of the terminal columns also being exposed to the outside beyond the resin encapsulate, each inner lead possessing a rectangular cross-section and having four surfaces including a

10

15

20

25

surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surf of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

According to another aspect of the present invention there is provided a resin-encapsulated semiconductor device using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of inner leads is less than that of the lead frame blank comprising: inner leads having the thickness less than that of the lead frame blank; and terminal columns integrally connected to the inner leads and having the same thickness with the lead frame blank, the terminal columns possessing a column-shaped configuration which is adapted to be electrically connected to an external circuit, the terminal columns being disposed outside of the inner leads in a manner such that they are coupled to the inner leads in a direction orthogonal to the thickness-wise direction thereof, portions of top ends of the terminal columns being exposed to the outside beyond a resin encapsulate, outer surfaces of the terminal columns also being exposed to the outside beyond the resin encapsulate, each inner lead

possessing a rectangular cross-section and having four surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

According to another aspect of the present invention, a semiconductor chip is received inward of the inner leads, and electrodes (pads) of the semiconductor chip are electrically connected to the inner leads through wires, respectively. According to another aspect of the present invention, the lead frame has a die pad, and the semiconductor chip is mounted onto the die pad. According to another aspect of the present invention, the lead frame does not have a die pad, and the semiconductor chip is fastened to the inner leads using a reinforcing fastener tape. According to still another aspect of the present invention, the semiconductor chip is fastened by means of insulating adhesive to the second surfaces of the inner leads on one surface thereof on which the electrodes are located, and the electrodes of the semiconductor chip are electrically connected to the first surfaces of the inner leads through wires, respectively. According to yet still

another aspect of the present invention, the semiconductor chip is fastened to the second surfaces of the inner leads by bumps thereby to be electrically connected to the inner leads. In the above descriptions, in the case that the terminal columns have terminal portions which are arranged on top ends of the terminal columns, with the terminal portions made of solders, etc. and exposed to the outside beyond the resin encapsulate, while it is the norm that the terminal portions comprising the solders, etc. are exposed to the outside beyond the resin encapsulate, it is not necessarily required for the terminal portions to be projected beyond the resin encapsulate. Moreover, while it is possible to use the outside surfaces of the terminal columns while they are not encapsulated by the resin encapsulate and they are exposed to the outside, the outside surfaces of the terminal columns which are not encapsulated by the resin encapsulate, can be covered by a protective frame using adhesive, etc.

## 20 [WORKING FUNCTIONS]

The resin-encapsulated semiconductor device in accordance with the present invention can meet a demand for an increase in the number of terminals. At the same time, in the resin-encapsulated semiconductor device, because the forming process of the outer leads as in the case of using

a mono-layered lead frame shown in FIG. 13(b) is not required, it is possible to provide a semiconductor device in which no problems are caused in association with position shift and coplanarity of the outer leads. More particularly, the use of a multi-pinned lead frame shaped in a manner that inner leads have a thickness less than that of the lead frame blank by a two-step etching process, that is, the inner leads are arranged at a fine pitch, can meet a demand for an increase in the pin number of the semiconductor device. Furthermore, by using the lead frame which is fabricated by a two-step etching process as will be described later with reference to FIG. 1, the second surface of each inner lead has coplanarity, and is excellent in wire-bonding property. In addition, since the first surface of the inner lead is also a flat surface and the third and fourth surfaces are depressed toward the inside of the inner lead, the inner leads are stable and coplanarity width upon wire bonding process can be enlarged.

#### [EMBODIMENTS]

Embodiments of the resin-encapsulated semiconductor device in accordance with the present invention will now be described with reference to the attached drawings. First, a resin-encapsulated semiconductor device in accordance



with a first embodiment of the present invention described hereinafter with reference to FIGS. 1. FIG. 1(a) is a cross-sectional view of the encapsulated semiconductor device according to the embodiment of the present invention. FIG. 1(b) is a sectional view of an inner lead taken along the line of FIG. 1(a), and FIG. 1(c) is a cross-sectional view of a terminal column taken along the line B1-B2 of FIG. 1(a). Moreover, FIG. 2(a) is a perspective view of the encapsulated semiconductor device according to the embodiment of the present invention, FIG. 2(b) is a top view of the resin-encapsulated semiconductor device of FIG. 2(a), and FIG. 2(c) is a bottom view of the encapsulated semiconductor device of FIG. 2(a). In FIGS. 1 and 2, a drawing reference numeral 100 represents a resin-encapsulated semiconductor device, 110 a semiconductor chip, 111 electrodes (pads), 120 wires, 130 a lead frame, 131 inner leads, 131Aa a first surface, 131Ab a second surface, 131Ac a third surface, 131Ad a fourth surface, 132 terminal columns, 133A terminal portions, 133B side surfaces, 133S a top surface, 135 a die pad, and 140 a resin encapsulate.

In the resin-encapsulated semiconductor device according to the first embodiment, as shown in FIG. 1, the semiconductor chip 110 is placed inward of the

leads 131. As can be readily seen from FIG. 1(a), the semiconductor chip 110 is mounted on the die pad 133 at one surface thereof which is opposed to the other surface thereof where the electrodes pads 111 of the semiconductor chip 110 are arranged. Each electrode pad 111 is electrically connected to the second surface 131Ab of the inner lead 131 through the wire 120. The electrical connection between the resin-encapsulated semiconductor device 100 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 100 via the terminal portions 133A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 133A located on the top surfaces 133S of the terminal columns 133, respectively. In the resin-encapsulated semiconductor device of the first embodiment of the present invention, it is not necessarily required to provide a protective frame 190, and instead, a structure, as shown in FIG. 1(d), in which no protective frame is used can be adopted.

The lead frame 130 used in the semiconductor device 100 according to the first embodiment is made of a 42% nickel-iron alloy. Therefore, the lead frame 130A which has a contour as shown in FIG. 9(a) and is shaped by an etching process, is used as the lead frame 130. The lead frame 130 has inner leads 131 which are shaped to have a

thickness less than that of the terminal columns 133 or other portions. Dam bars 136 serve as a dam when encapsulating the semiconductor chip 110 with a resin. Moreover, although the lead frame 130A which is processed by etching to have the contour as shown in FIG. 9A is used in this embodiment, the lead frame is not limited to such a contour because portions except the inner leads 131 and the terminal columns 133 are not necessary. The inner leads 131 have a thickness of 40  $\mu$ m whereas the portions of the lead frame 130 other than the inner leads 131 have a thickness of 0.15 mm which corresponds to the thickness of the lead frame blank. The other portions of the lead frame 130 except the inner leads 131 may not have the thickness of 0.15 mm, but have a thickness of 0.125 mm-0.50 mm which is thinner. The tips of the inner leads 131 have a small pitch of 0.12 mm so as to achieve an increase in the number of terminals for semiconductor devices. The second face 131Ab of the inner lead 131 has a substantially flat profile so as to allow an easy wire bonding thereon. Also, as shown in FIG. 1(b), because the third and fourth faces 131Ac and 131Ad have a concave shape which is depressed toward the inside of the associated inner lead, a high strength can be obtained even though the second face (wire bonding surface) 131Ab is narrowed.

In the present embodiment, since twisting does not

occur in the inner leads 131 irrespective of whether the inner leads 131 is long or not. The inner leads having the contour, as shown in FIG. 9(a), in which the tips of the inner leads 131 are separated one from another, are prepared by the etching process, and the inner leads are resin-encapsulated after mounting the semiconductor chip thereon as will be described later. However, where the inner leads 131 are long in their length and have a tendency for the generation of twisting therein, it is impossible to fabricate the lead frame by etching to have the contour as shown in FIG. 9(a). Therefore, after etching the lead frame in a state where the tips of the inner leads are fixed to the connecting portion 131B as shown in FIG. 9(c)(1), the inner leads 131 are fixed with the reinforcing tape 160 as shown in FIG. 9(c)(2). Then, the connecting portions 131B which are not necessary in the fabrication of the resin-encapsulated semiconductor device are removed by a press as shown in FIG. 9(c)(3), and a semiconductor device is then mounted on the lead frame.

Hereinafter, a method for the fabrication of the resin-encapsulated semiconductor device will now be described with reference to FIG. 8. First, the lead frame 130A, as shown in FIG. 9(a), which is shaped by the etching process as will be described later, is prepared such that the second surfaces 131Ab of the inner leads 131 are

directed upward (FIG. 8(a)).

Then, the semiconductor chip 110 is mounted onto the die pad 135 such that the surfaces of the semiconductor chip 110 on which the electrodes 111 are arranged, are  
5 directed upward (FIG. 8(b)).

Next, after the semiconductor chip 110 is fastened onto the die pad 135, the electrodes 111 of the semiconductor chip 110 and the second surfaces 131ab of the inner leads 131 are bonded with each other using wires 120  
10 (FIG. 8(c)).

Subsequently, encapsulation is carried out with the conventional resin encapsulate 140. Thereafter, unnecessary portions of the lead frame 130 which are protruded from the resin encapsulate 140 are cut by a press  
15 to form terminal columns 133 and also the side surfaces 133b of the terminal columns 133 (FIG. 8(d)).

Then, the dam bars 136, the frame portions 137, etc. of the lead frame 130A as shown in FIG. 9 are removed. Next, the terminal portions 133A each made of the semi-spherical solder are arranged on the outer surface of each  
20 terminal column 133 to fabricate a resin-encapsulated semiconductor device (FIG. 8(e)).

Thereafter, the protective frame 180 is arranged by means of adhesive around an entire outer surface of the  
25 resultant structure in such a manner that the side surfaces

of the terminal columns 133 are covered thereby FIG. 6(f)). At this time, the protective frame 180 functions to reinforce the semiconductor device. In other words, the protective frame 180 serves to prevent moisture from  
5 leaking into a gap between the resin encapsulate and the terminal columns due to the fact that the side surfaces of the terminal columns are exposed to the outside, whereby a crack is not formed in the semiconductor device and the breakage of the semiconductor device is avoided. However,  
10 persons skilled in the art will readily appreciate that it is not necessarily required to provide the protective frame 180. Also, when such an encapsulating process by the resin is carried out using a desired mold, the encapsulating process is implemented in a state wherein the outer side  
15 surfaces of the terminal columns of the lead frame are somewhat protruded out of the resin encapsulate.

A method for etching the lead frame of the first embodiment will now be described in conjunction with the attached drawings. FIG. 11 is of cross-sectional views  
20 respectively illustrating sequential steps of the etching process for the lead frame of the first embodiment. In particular, the cross-sectional views of FIG. 1 correspond to a cross section taken along the line D1-D2 of FIG. 9(a). In FIG. 11, the reference numeral 1110 denotes a lead frame  
25 blank, 1120A and 1120B resist patterns, 1130 first opening,

1140 second openings, 1150 first concave portions, 1160 second concave portions, 1170 flat surfaces, and 1180 an etch-resistant layer. First, a water-soluble casein resist using potassium dichromate as a sensitive agent is coated  
5 over both surfaces of the lead frame blank 1110 made of a 42% nickel-iron alloy and having a thickness of about 0.15 mm. Using desired pattern plates, the resist films are patterned to form resist patterns 1120A and 1120B having first opening 1130 and second openings 1140, respectively  
10 (FIG. 11(a)).

The first opening 1130 is adapted to etch the lead frame blank 1110 to have a flat etched bottom surface to a thickness smaller than that of the lead frame blank 1110 in a subsequent process. The second openings 1140 are adapted  
15 to form desired shapes of tips of inner leads. Although the first opening 1130 includes at least an area forming the tips of the inner leads 1110, a topology generated by partially thinned portion by etching in a subsequent process can cause hindrance in a taping process or a  
20 clamping process for fixing the lead frame. Thus, an area to be etched needs to be large without being limited to fine portions of the tips of the inner leads. Thereafter, both surfaces of the lead frame blank 1110 formed with the resist patterns are etched using a 48 Be' ferric chloride  
25 solution of a temperature of 57°C at a spray pressure of

2.5 kg/cm<sup>2</sup>. The etching process is terminated at the point of time when first recesses 1150 etched to have a flat etched bottom surface have a depth  $h$  corresponding to  $1/3$  of the thickness of the lead frame blank (FIG. 11a).

5 Although both surfaces of the lead frame blank 1110 are simultaneously etched in the primary etching process, it is not necessary to simultaneously etch both surfaces of the lead frame blank 1110. The reason why both surfaces of the lead frame blank 1110 are simultaneously etched, as in  
10 this embodiment, is to reduce the etching time taken in a secondary etching process as will be described later. The total time taken for the primary and secondary etching processes is less than that taken in the case of etching of only one surface of the lead frame blank on which the  
15 resist pattern 1120B is formed. Subsequently, the surface provided with the first recesses 1150 respectively etched at the first opening 1130 is entirely coated with an etch-resistant hot-melt wax (acidic wax type MR-WB6, The Inctec Inc.) by a die coater to form an etch-resistant  
20 layer 1180 so as to fill up the first recesses 1150 and to cover the resist pattern 1120A (FIG. 11(c)).

It is not necessary to coat the etch-resistant layer 1180 over the entire portion of the surface provided with the resist pattern 1120A. However, it is preferred that  
25 the etch-resistant layer 1180 be coated over the entire



portion of the surface formed with the first recesses and first opening 1130, as shown in FIG. 11(c), because it is difficult to coat the etch-resistant layer 1180 on the surface portion including the first recesses.

5 Although the etch-resistant layer 1180 wax employed in this embodiment is an alkali-soluble wax, any suitable wax resistant to the etching action of the etchant solution remaining somewhat soft during etching may be used.

for forming the etch-resistant layer 1180 is not limited to the above-mentioned wax, but may be a wax of a UV-se type. Since each first recess 1150 etched by the pre-etching process at the surface formed with the pattern is adapted to form a desired shape of the inner lead to be filled up with the etch-resistant layer 1180, it is

10 further etched in the following secondary etching process. The etch-resistant layer 1180 also enhances the mechanical strength of the lead frame blank for the second etching process, thereby enabling the second etching process to be conducted while keeping a high accuracy. It is

15 possible to enable a second etchant solution to be sprayed at an increased spraying pressure, for example, 2.5 kg or above, in the secondary etching process. The increased spraying pressure promotes the progress of etching in the direction of the thickness of the lead frame blank in the secondary etching process. Then, the lead frame blank

20

25

subjected to a secondary etching process. In this secondary etching process, the lead frame blank 1110 is etched at its surface formed with first recesses 1150 having a flat etched bottom surface, to completely  
5 perforate the second recesses 1160, thereby forming the tips of inner leads 131A (FIG. 11(d)).

The bottom surface 1170 of each recess formed by the primary etching process is flat. However, both side surfaces of each recess positioned at opposite sides of the  
10 bottom surface 1170 have a concave shape depressed toward the inside of the inner lead. Then, the lead frame blank is cleaned. After completion of the cleaning process, the etch-resistant layer 1180, and resist films (resist patterns 1120A and 1120B) are sequentially removed. Thus,  
15 a lead frame 130A having a structure of FIG. 9(a) is obtained in which tips of the inner leads 131A are arranged at a fine pitch. The removal of the etch-resistant layer 1180 and resist films (resist patterns 1120A and 1120B) is achieved using a sodium hydroxide solution serving to  
20 dissolve them.

The processes for manufacturing the lead frame as shown in FIG. 11, is to form by means of etching the lead frame having the tips of the inner leads used in this  
25 embodiment of the present invention, which have a thickness less than that of the lead frame. Especially, the first

surfaces 131Aa of the tips of the inner leads as shown in  
FIG. 1, are flushed with one surfaces of remaining portions  
of the inner leads having the same thickness with the lead  
frame while being opposed to the second surfaces 131Ab, and  
5 the third and fourth surfaces are formed to have a concave  
shape which is depressed toward the inside of the inner  
leads. Where a semiconductor chip is mounted on the second  
surfaces 131Ab of the inner leads by means of bumps for an  
electrical connection therebetween, as in a semiconductor  
10 device according to a third embodiment as will be described  
hereinafter, an increased tolerance for the connection by  
bumps is obtained when the second surface 131Ab has a  
concave shape depressed toward the inside of the inner  
lead. To this end, an etching method shown in FIG. 12 is  
15 adopted in this case. The etching method shown in FIG. 12  
is the same as that of FIG. 11 in association with its  
primary etching process. After completion of the primary  
etching process, the etching method is conducted in a  
manner different from that of the etching method of FIG. 11  
20 in that the second etching process is conducted at the side  
of the first recesses 1150 after filling up the second  
recesses 1160 by the etch-resist layer 1180, thereby  
completely perforating the second recesses 1160. At this  
time, by implementing the primary etching process, etching  
25 at the side of the second openings 1140 is performed in a

sufficient manner. The cross section of each inner lead, including its tip, formed in accordance with the etching method of FIG. 12, has a concave shape depressed toward the inside of the inner lead at the second surface 131Ab, as shown in FIG. 6(b).

The etching method in which the etching process is conducted at two separate steps, respectively, as in that of FIGs. 11 and 12, is generally called a "two-step etching method". This etching method is advantageous in that a desired fineness can be obtained. The etching method used to fabricate the lead frame 130A of the first embodiment shown in FIG. 9 involves the two-step etching method and the method for forming a desired shape of each lead frame portion while reducing the thickness of each pattern formed. In particular, the etching method makes it possible to achieve a desired fineness. In accordance with the method illustrated in FIGs. 11 and 12, the fineness of the tip of each inner lead 131A formed by this method is dependent on the shape of the second recesses 1160 and the thickness  $t$  of the inner lead tip which is finally obtained. For example, where the blank has a thickness  $t$  reduced to 50  $\mu\text{m}$ , the inner leads can have a fineness corresponding to a lead width  $W_1$  of 100  $\mu\text{m}$  and a tip pitch  $p$  of 0.15 mm, as shown in FIG. 11(e). In the case of using a small blank thickness  $t$  of about 30  $\mu\text{m}$  and a lead

width  $W_1$  of 70  $\mu\text{m}$ , it is possible to form inner leads having a fineness corresponding to an inner lead pitch  $p$  of 0.12 mm. Of course, it may be possible to form inner leads having a further reduced tip pitch by adjusting the blank thickness  $t$  and the lead width  $W_1$ . That is to say, an inner lead tip pitch  $p$  up to 0.08 mm, a blank thickness up to 25  $\mu\text{m}$ , and a lead width  $W_1$  up to 40  $\mu\text{m}$  can be obtained.

In the case where twisting of the inner leads does not occur in the fabricating process, as in the case where the inner leads are short in their length, a lead frame illustrated in FIG. 9(a) can be directly obtained. However, where the inner leads are long in length as compared to those of the first embodiment, the inner leads have tendency for the generation of twisting. Thus, in this case, the lead frame is obtained by etching in a state where the tips of the inner leads are bound to each other by a connecting member 131B as shown in FIG. 9(c)(1). Then, the connecting member 131B which is not necessary for the fabrication of a semiconductor package is cut off by means of a press to obtain a lead frame shaped as shown in FIG. 9(a).

Moreover, as described above, where unnecessary portions in a structure shown in FIG. 9(c)(1) are cut to obtain the lead frame having the contour shown in FIG.

9(a), a reinforcing tape 160 (a polyimide tape is generally used, as shown in FIG. 9(c)(A)). While the connecting member 131B is cut off by means of a press to obtain the contour shown in FIG. 9(c)(D), a semiconductor device is mounted on the lead frame still having the reinforcing tape attached thereon. Also, the mounted semiconductor device is encapsulated with a resin in a condition where the lead frame still has the tape. The line E11-E12 illustrates a cut portion.

The tip of the inner lead 131 of the lead frame used in the semiconductor device of this first embodiment has a cross-sectional shape as shown in FIG. 13(1)(a). The tip 131A has an etched flat surface (second surface) 131Ab which is substantially flat and therefore has a width  $W1$  slightly greater than the width  $W2$  of an opposite surface. The widths  $W1$  and  $W2$  (about 1000  $\mu\text{m}$ ) are more than the width  $W$  at the central portion of the tips when viewed in the direction of the inner lead thickness. Thus, the tip of the inner lead has a cross-sectional shape having opposite wide surfaces. To this end, although either of the opposite surfaces of the tip 131A can be easily electrically connected to a semiconductor device (not shown) by a wire 120A or 120B, this embodiment illustrates the use of the etched flat surface for wire-bonding as shown in FIG. 13(D)(a). In FIG. 13, a reference numeral

131Ab depicts an etched flat surface, 131Aa a surface of a lead frame blank, and 121A and 121B, respectively, a plated portion. In the case of FIG. 13(Δ)(a), there has particularly excellent in wire-bonding property, because the etched flat surface does not have roughness. FIG. 13(Δ) shows that the tip 1331B of the inner lead of the lead frame fabricated according to the process illustrated in FIG. 14 is wire-bonded to a semiconductor device. In this case, however, both the opposite surfaces of the tip 1331B of the inner lead are flat, but have a width smaller than that in a direction of the inner lead thickness. In addition to this, as both the opposite surfaces of the tip 1331B is formed of surfaces of the lead frame blank, these surfaces have an inferior wire-bonding property as compared to that of the etched flat surface of this first embodiment. FIG. 13(=) shows that the inner lead tip 1331C or 1331D, obtained by thinning in its thickness by a means of a press (coining) and then by etching, is wire-bonded to a semiconductor device (not shown). In this case, however, a pressed surface of the inner lead tip is not flat as shown FIG. 13(=). Thus, the wire-bonding on either of the opposite surfaces as shown in FIG. 13(=)(a) or FIG. 13(=)(b) often results in an insufficient wire-bonding stability and a problematic quality. The drawing reference numeral 1331Ab represents a coining surface.

A modified example of the resin-encapsulated semiconductor device in accordance with the first embodiment of the present invention will be described hereinafter. FIGs. 3(a) through 3(e) are cross-sectional views of the modified example of the resin-encapsulated semiconductor device in accordance with the first embodiment of the present invention. The semiconductor device of the modified example as shown in FIG. 3(a), is different from that of the first embodiment in that a position of the die pad 135 is changed, that is, the die pad 135 is exposed to the outside. By the fact that the die pad 135 is exposed to the outside, the heat dissipation property is improved as compared to the first embodiment. Also, in the semiconductor device of the modified example as shown in FIG. 3(b), because the die pad 135 is exposed to the outside, the heat dissipation property is improved as compared to the first embodiment. Unlike the first embodiment or the modified example as shown in FIG. 3(a), in the present modified example as shown in FIG. 3(b), because a direction of the semiconductor device 110 is changed, the first surfaces of the lead frame are established as the wire bonding surfaces. The modified examples as shown in FIGs. 3(c), 3(d) and 3(e), illustrate semiconductor devices which are obtained by modifying the semiconductor devices of the first embodiment, the modified



example as shown in FIG. 3(a) and the modified example as shown in FIG. 3(b), wherein the semi-spherical solders are not used, and instead, the top surfaces of the terminal columns are directly used as the terminal portions, whereby  
5 an entire manufacturing procedure can be simplified.

Next, a resin-encapsulated semiconductor device in accordance with a second embodiment of the present invention will be described. FIG. 4(a) is a cross-sectional view of the resin-encapsulated semiconductor  
10 device in accordance with the second embodiment of the present invention, FIG. 4(b) is a cross-sectional view illustrating inner leads, taken along the line A3-A4 of FIG. 4(a), and FIG. 4(c) is a cross-sectional view illustrating a terminal column, taken along the line B3-B4  
15 of FIG. 4(a). Because an outer appearance of the semiconductor device of the second embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 3, the drawing reference numeral 200 represents a semiconductor device,  
20 210 a semiconductor chip, 211 electrodes (pads), 220 wires, 230 a lead frame, 231 inner leads, 231Ab a second surface, 231Ac a third surface, 231Ad a fourth surface, 233 terminal columns, 233A terminal portions, 233B side surfaces, 233S top surfaces, 240 a resin encapsulate, and 270 a  
25 reinforcing fastener tape. In the semiconductor device of

this second embodiment, the lead frame 230 does not have a die pad, the semiconductor chip 210 is fastened to the inner leads 231 by the reinforcing fastener tape 270, and the semiconductor chip 210 is electrically connected at its electrodes (pads) 211 to the second surfaces 231ab of the inner leads 231 by wires 220. Also, in the case of this second embodiment, similarly to the first embodiment, the electrical connection between the resin-encapsulated semiconductor device 200 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 200 via the terminal portions 233A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 233A located on the top surfaces 233S of the terminal columns 233, respectively.

In addition, the semiconductor device of this second embodiment does not have a die pad as shown in FIGs. 10(a) and 10(b). The manufacturing method of the semiconductor device of this embodiment using the lead frame 230A which is shaped by the etching process is substantially the same as that of the first embodiment except that, while in the case of the first embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip is fastened to the inner leads, in the case of the second embodiment, the wire

bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip 210 is fastened together with the inner leads 231 by the reinforcing fastener tape 270. Also, the cutting process for the unnecessary portions and the terminal portion forming process after resin encapsulating process are implemented in the same way as the first embodiment. The lead frame 230 as shown in FIG. 10(a) is obtained in the same manner by which the lead frame 130A as shown in FIG. 9(a) is obtained. In other words, by cutting the resultant structure obtained after etching the structure as shown in FIG. 10(c)(1), the contour as shown in FIG. 10(a) is obtained. At this time, the conventional reinforcing fastener tape 260 (the polyimide tape) as shown in FIG. 10(c)(2), which performs a reinforcing function is used.

FIG. 5(a) through 5(c) are cross-sectional views illustrating modified examples of the semiconductor device of the second embodiment. The semiconductor device as shown in FIG. 5(a) is different from the semiconductor device of the second embodiment, in that the surface of the semiconductor chip thereof which has the electrodes is directed downward. The modified examples as shown in FIGS. 5(b) and 5(c), illustrate semiconductor devices which are obtained by modifying the semiconductor devices of the second embodiment and the modified example as shown in FIG.

5(a), wherein the semi-spherical solders are not used, and instead, the top surfaces of the terminal columns are directly used as the terminal portions. In these examples, because a protective frame is not used and the side surfaces 233B of the terminal columns 333 are exposed to the outside, a checking operation by a test, etc. can be easily performed.

Hereinafter, a resin-encapsulated semiconductor device in accordance with a third embodiment of the present invention will be described. FIG. 6(a) is a cross-sectional view of the resin-encapsulated semiconductor device of the third embodiment, FIG. 6(b) is a cross-sectional view illustrating inner leads, taken along the line A5-A6 of FIG. 6(a), and FIG. 6(c) is a cross-sectional view illustrating a terminal column, taken along the line B5-B6 of FIG. 6(b). Because an outer appearance of the semiconductor device of the this third embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 6, the drawing reference numeral 300 represents a semiconductor device, 310 a semiconductor chip, 312 bumps, 330 a lead frame, 331 inner leads, 331Aa a first surface, 331Ab a second surface, 331Ac a third surface, 331Ad a fourth surface, 333 terminal columns, 333A terminal portions, 333B side surfaces, 333S top surfaces, 340 a resin encapsulate, and 350 a

reinforcing fastener tape. In the semiconductor device of this third embodiment, the semiconductor chip 310 is fastened to the second surfaces 331Ab of the inner leads 331 by the bumps 311 thereby to be electrically connected to the second surfaces 331Ab. The lead frame 330 has a contour as shown in FIGs. 10(a) and 10(b), which is formed by the etching process of FIG. 11. As shown in FIG. 13(1)(b), both widths W1A and W2A (about 100  $\mu$ m) at top and bottom ends of the inner leads 331 are larger than a width WA at a center portion in a thickness-wise direction. Due to the fact that the second surfaces 331Ab of the inner leads 331 is depressed toward the inside of the inner leads and the first surfaces 331Aa are flat, a desired fineness can be obtained. Also, when the second surfaces 331Ab of the inner leads 331 are electrically connected to the semiconductor chip via bumps, easy connection can be accomplished as shown in FIG. 13(2)(b). Further, in the case of this third embodiment, as in the case of the first and second embodiments, the electrical connection between the resin-encapsulated semiconductor device 300 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 300 via the terminal portions 333A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 333A located on the top surfaces of the terminal

columns 333, respectively.

5 In addition, unlike the semiconductor device of the first embodiment, the semiconductor device of this third embodiment uses a lead frame which is shaped by the etching process as shown in FIG. 12. However, the manufacturing method of the semiconductor device of this embodiment is substantially the same as that of the first embodiment except that, while in the case of the first embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip is fastened to the inner leads, in the case of this third embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip 310 is fastened to the inner leads 331 via the bumps. Also, the cutting process for the unnecessary portions and the terminal portion forming process after resin encapsulating process are implemented in the same way as the first embodiment.

20 FIG. 6(d) is a cross-sectional view illustrating a modified example of the semiconductor device in accordance with the third embodiment of the present invention. In the modified example of the semiconductor device as shown in FIG. 6(d), the terminal portions each comprising the semi-spherical solder are not provided, and the top surfaces of the terminal columns are directly used as the terminal

portions. Because the protective frame is not used and the side surfaces 333B of the terminal columns 333 are exposed to the outside, a checking operation by a test, etc. can be easily performed.

5           Hereinafter, a resin-encapsulated semiconductor device in accordance with a fourth embodiment of the present invention will be described. FIG. 7(a) is a cross-sectional view of the resin-encapsulated semiconductor device of the fourth embodiment, FIG. 7(b) is a cross-sectional view illustrating inner leads, taken along the line A7-A8 of FIG. 7(a), and FIG. 7(c) is a cross-sectional view illustrating a terminal column, taken along the line B7-B8 of FIG. 7(b). Because an outer appearance of the semiconductor device of the this fourth embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 7, the drawing reference numeral 400 represents a semiconductor device, 10       410 a semiconductor chip, 411 pads, 430 a lead frame, 431 inner leads, 431Aa a first surface, 431Ab a second surface, 431Ac a third surface, 431Ad a fourth surface, 433 terminal columns, 433A terminal portions, 433B side surfaces, 433S top surfaces, 440 a resin encapsulate, and 470 insulating adhesive. In the semiconductor device of this fourth embodiment, one surface of the semiconductor chip 410 on which the pads 411 are disposed is fastened to the second  
15  
20  
25

surfaces 431Ab of the inner leads 431 by the insulating  
adhesive 470, and the pads 411 and the first surfaces  
of the inner leads 431 are electrically connected with  
other by wires 420. The semiconductor device of  
5 fourth embodiment uses the same lead frame which is used  
the third embodiment, which has the contour as shown  
FIG. 10(a) and 10(b). Also, in the case of this fourth  
embodiment, as in the case of the first and second  
embodiments, the electrical connection between the res  
10 encapsulated semiconductor device 400 of this embodiment  
and an external circuit is achieved by mounting the res  
encapsulated semiconductor device 400 via the terminal  
portions 433A each being made of a semi-spherical solder  
on a printed circuit substrate, with the terminal portions  
15 433A located on the top surfaces of the terminal columns  
433, respectively.

FIG. 7(d) is a cross-sectional view illustrating  
a modified example of the semiconductor device in accordance  
with the fourth embodiment of the present invention. In  
20 the modified example of the semiconductor device as shown  
in FIG. 7(d), the terminal portions each comprising the  
semi-spherical solder are not provided, and the top  
surfaces of the terminal columns are directly used as the  
terminal portions. Because the protective frame is not  
25 used and the side surfaces 433B of the terminal columns 433



are exposed to the outside, a checking operation by a test, etc. can be easily performed.

#### (EFFECTS OF THE INVENTION)

5 The present invention provides a resin-encapsulated semiconductor device employing the above-mentioned lead frame, which is capable of meeting a demand for the increased terminal number. Furthermore, the resin-encapsulated semiconductor device in accordance with this invention does not require a process of cutting or bending the dam bars as in the case of using a lead frame having outer leads as shown in FIG. 13(b). As a result of this, the resin-encapsulated semiconductor device does not have a problem in that the outer leads are bent, or a problem associated with coplanarity. In addition to these advantages, the resin-encapsulated semiconductor device has a shortened interconnection length as compared to the QTP or the BGA, whereby the semiconductor device can be reduced in a parasitic capacity, and shortened in a transfer delay time.

59:543 v1

59:543 v1

特開平 9-8205

(13) 公報日 平成 9 年 (1997) 1 月 13 日

(51) Int. Cl.

H01L 23/56

発明の名称

発明の要約

F 1

H01L 23/56

特許表示

13/12

13/12

審査請求 異議 再審査請求 F D (全 1 頁)

(11) 出願番号 特願 7-170490

(12) 出願日 平成 7 年 (1995) 6 月 14 日

(11) 出願人 000002897

大日本印刷株式会社

東京都新宿区市谷加賀町一丁目 1 号

(12) 発明者 山田 成一

東京都新宿区市谷加賀町一丁目 1 号

大日本印刷株式会社内

(13) 発明者 佐々木 賢

東京都新宿区市谷加賀町一丁目 1 号

大日本印刷株式会社内

(14) 代理人 弁護士 小西 康典

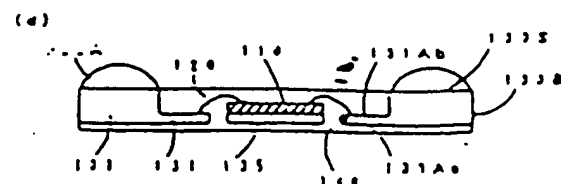
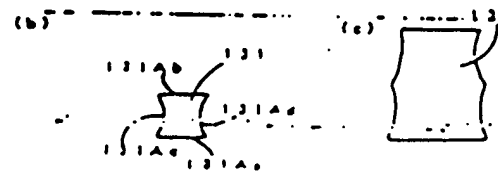
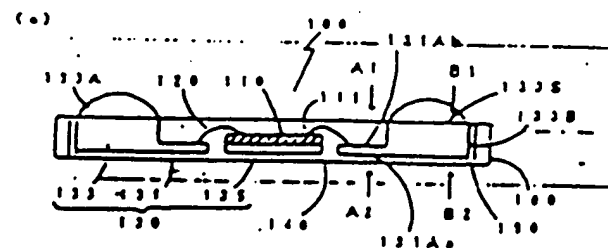
(54) (発明の名称) 断層防止型半導体装置

(57) (要約)

(発明者)

【目的】 多素子化に対応でき、且つ、アフターリードの位置ズレや平坦性の問題にも対応できる断層防止型半導体装置を提供する。

【構成】 一体的に製造したリードフレーム素子と同一部をの外部回路と接続するための接続の端子部 133 とを有し、且つ、端子部はインナーリードの外側にあり、インナーリードに対して厚み方向に突出して設けられており、端子部の先端面に半田等からなる端子部を設け、端子部を断層防止部から突出させ、端子部の外部側の側面を断層防止部から突出させており、インナーリードは、断面形状が略方形で第 1 面 131Aa、第 2 面 131Ab、第 3 面 131Ac、第 4 面 131Ad の 4 面を有しており、かつ第 1 面はリードフレーム素子と同じ部をの地の部分の一方の面と同一平面上にあり、第 2 面に向合っており、第 3 面、第 4 面はインナーリードの内側に向かって凹んだ形状に形成されている。



(4) 計算式の整理

(図2項1) 2 段ニッチング加工によりインナーリードの厚さがリードフレーム素材の厚さよりも厚大に形成されたリードフレームを用いた半導体装置であつて、前記リードフレームは、リードフレーム素材よりも厚大のインナーリードと、該インナーリードに一体的に連結したリードフレーム素材と同じ厚さの外側図柄とを形成するための柱状の端子柱とを有し、且つ、端子柱はインナーリードの外周面においてインナーリードに対して厚さ方向に傾斜して設けられており、端子柱の先端部に半導体からなる端子部を設け、端子部を防止層層部から露出させ、端子柱の外周側の側面を防止層層部から露出させており、インナーリードは、断面形状が矩形で第1面、第2面、第3面、第4面の4面を有しており、かつ第1面はリードフレーム素材と同じ厚さの他の部分の一方の面と同一直線上にあつて第2面に向合っており、第3面、第4面はインナーリードの内側に向かつて凹んだ形状に形成されていることを外面とする層部防止層を有する。

〔実施例2〕 2枚エッチング板によりインターリードの板をリードフレーム基板上の板より厚肉板に形成加工されたリードフレームを用いた半導体装置であつて、前記リードフレームは、リードフレーム基板上より厚肉のインターリードと、該インターリードに一体的に連結したリードフレーム基材と同じ厚さの外縁面側と形成するための形状の導子柱とを有し、且つ、導子柱はインターリードの外縁側においてインターリードに対して厚み方向に直交して設けられており、導子柱の先端の一部を封止用樹脂層から露出させて導子柱とし、導子柱の外縁側の側面を封止用樹脂層から露出させており、インターリードは、断面形状が矩形で第1面、第2面、第3面、第4面の4面を有しており、かつ第1面はリードフレーム基材と同じ厚さの他の面分の一方の面と同一平面上にあって第2面に向き合っており、第3面、第4面はインターリードの内側に向かつて凹んだ形状に形成されていることを特徴とする所記封止型半導体装置。

(図 5 第 3) 加減算しないし 2 において、半導体素子はインナーリード間に設けられ、該半導体素子の電極部はワイヤにてインナーリードと電気的に接続されていることを特徴とする増設防止型半導体装置。

(請求項4) 請求項3において、リードフレームにダイパッドを有しており、半導体素子にダイパッド上に搭載され、固定されていることも特徴とする発明は、請求項4を構成する。

(2) 部品 5) は部品 3) において、リードフレームはダイパッドを溶けないもので、半導体素子はインナーリードとともに高強度固定テープにより固定されていることを特徴とする新規防止型半導体装置。

(註文項6) 注文項1ないし2において、半紙3枚を  
1枚半紙枚数の電圧調整の面をインナーリードの第2面

に池田政雄氏により鑑定されており、該本と本館蔵の  
二部はワイナによりインナーリードの同一部と見做さ  
れ、部数に差があることを確認する書指対照型本と見  
做す。

(図5-7) 図5-6の1ないし2において、主風管系はパンプによりインターリードの第2区に固定されて空気にインターリードと接続していることを示唆とする。本設計は主風管系である。

(月 廿 二 日 午 時 分 刻)

( 0 0 0 1 )

（構造上の利用分岐）本系列は、半導体装置の多岐多化に対応して、主として、アフターリードの位置ズレ（スニュー）やアフターリードの非恒性（コブラアリティィ）の低減に効果的で、リードフレームを用いた新増設止型半導体装置に於ける。

( 0 0 0 2 )

(従来の型) 従来のより用いられている標準型のは  
ほぼ8倍 (プラスチックリードフレームパッケージ)

は、一面に図15(1)に示されるような構造であり、半導体素子1520を格納するダイパッド部1511の両面の区域との電気的接続を行うためのアフターリード部1513、アフターリード部1513に一体となったインナーリード部1512、該インナーリード部1512の先端部と半導体素子1520の電極パッド1521とを電気的に接続するためのワイヤ1530、半導体素子1520を封止して外界からの応力、汚染から守る樹脂1540面からなっており、半導体素子1520をリードフレームのダイパッド1511区域に格納した場合には、樹脂1540により封止してパッケージとしたもので、半導体素子1520の電極パッド1521に対応する数のインナーリード1512を必要とするものである。そして、このような樹脂封止型の半導体素子の絶縁膜リフトして取られる（暴露）リードフレームは、一面には図15(b)に示すような構造のもので、半導体素子を格納するためのダイパッド1511と、ダイパッド1511の周囲に設けられた半導体素子と格納するためのインナーリード1512、該インナーリード1512に連通して外部接続との電気を行うためのアフターリード1513、樹脂封止する膜のダムとなるダムバー15

10 14. リードフレーム1510全体を支持するフレーム  
(E)は、図1515Eを備えており、通孔、コパール、4  
2を含む(42×ニッケル-6を含む)、鉄板を含むような  
導電性に優れた金属を用い、プレス加工もしくはエッチン  
グ法により形成されていた。図15(b)(c)  
は、図15(c)(i)に示すリードフレーム基盤図の  
F1-F2における断面図である。

〔000〕このようなリードフレームを削減した増設  
防止型の本装置は、ス（プラステックリードフレームパッ  
ッケージ）において、電子回路の収容密度の増大と  
品質の向上に、小型化かつ高信頼性の



(1)

特許第9-8205

面、第2面、第3面、第4面の4面を有しており、かつ第1面はリードフレーム基材と同じ広さの他の部分の一方の面と同一平面上にあって第2面に向き合っており、第3面、第4面はインナーリードの内側に向かって凹んだ形状に形成されていることを特徴とするものである。また、本発明の半導体装置は、2段エッチング加工によりインナーリードの底面がリードフレーム基材の底面よりも深部に形成加工されたリードフレームを用いた半導体装置であって、前記リードフレームは、リードフレーム基材よりも厚手のインナーリードと、インナーリードに一体的に形成したリードフレーム基材と同じ広さの外周部とを有するための形状の導電性を有し、且つ、導電性はインナーリードの外周部においてインナーリードに対して厚み方向に連続して設けられており、導電性の外周部の一部を禁止層層から露出させて導電性とし、導電性の外周部の側面を禁止層層から露出させており、インナーリードは、前記導電性が第1面、第2面、第3面、第4面の4面を有しており、かつ第1面はリードフレーム基材と同じ広さの他の部分の一方の面と同一平面上にあって第2面に向き合っており、第3面、第4面はインナーリードの内側に向かって凹んだ形状に形成されていることを特徴とするものである。そして、上記において、半導体素子は、インナーリードの底面に収まり、半導体素子の電極部(パッド)はワイヤにてインナーリードと電気的に接続されていることを特徴とするものである。また、前記リードフレームはダイパッドを有し、半導体素子はダイパッド上に形成、固定されていることを特徴とするものであり、前記リードフレームはダイパッドを有さないもので、半導体素子はインナーリードとともに弾性用テープにより固定されていることを特徴とするものである。また、上記において、リードフレームはダイパッドを有さないもので、半導体素子はインナーリードとともに弾性用テープにより固定されていることを特徴とするものである。また、上記において、半導体素子は、半導体素子の電極部(パッド)の底面をインナーリードの第2面に弾性層層により固定されており、前記半導体素子の電極部(パッド)はワイヤによりインナーリードの第1面に電気的に接続されていることを特徴とするものである。また、上記において、半導体素子は、パンプによりインナーリードの第2面に固定され、電気的にインナーリードと接続されていることを特徴とするものである。また、上記において、導電性の外周部に半導体からなる導電性を有し、導電性を禁止層層から露出させる場合、半導体からなる導電性は禁止層層から露出したものが一般的であるが、必ずしも露出する必要はない。また、導電性の外周部の側面を禁止層層から露出させて、その導電性を導電性を介して導電性としても良い。(0008)

(作用) 本発明の半導体装置は、上記のように構成することにより、リードフレームを用いた半導体装置において、多層化に対応でき、且つ、従来の図1(b)に示す半導体リードフレームを用いた場合のように、フッターリードのフォーミング工程を必要としないため、これらの工程に起因して発生していたフッターリードのスニューの問題やフッターリードの二重化(コープラティビティ)の問題を全く無くすることができ半導体装置の信頼性を高め得るものである。詳しくは、2段エッチング加工によりインナーリードの底面が基材の底面よりも深部に形成加工された、即ち、インナーリードを底面に加工された多ピン型のリードフレームを用いることにより、半導体装置の多層化に対応できるものとしている。更に、前述する、図1に示す2段エッチングにより形成された、リードフレームを用いることにより、インナーリード部の第2面は平坦性を確保でき、ワイヤボンディング性の良いものとしている。また第1面も平坦面で、第3面、第4面はインナーリード部に凹みであるためインナーリード部は、固定されており、且つ、ワイヤボンディングの平坦性を広くとれる。(0009)

(実施例) 本発明の半導体装置の具体的な実施例を図1に示して説明する。先ず、実施例1の半導体装置を図1(a)に示す。図1(a)は実施例1の半導体装置の断面図であり、図1(b)は図1(a)のA1-A2におけるインナーリード部の断面図で、図1(c)は図1(a)のB1-B2における導電性部の断面図で、図2(a)は実施例1の半導体装置の平面図であり、図2(b)はその正面図を、図2(c)は下面図を示している。図1、図2中、100は半導体素子、110は半導体素子の電極部(パッド)、120はワイヤ、130はリードフレーム、131はインナーリード、131Aは第1面、131Abは第2面、131Acは第3面、131Adは第4面、131Bは導電性部、131Aは電極部、131Bは側面、131Sは外周部、131Sはダイパッド、140は禁止層層である。本実施例1の半導体装置においては、図1(a)に示すように、半導体素子100は、インナーリード131に収まり、且つ、半導体素子は、図1(a)で半導体素子100の電極部(パッド)111を上にし、半導体素子100の電極部(パッド)111の底面をインナーリード131の第2面131Abにてワイヤ120により、電気的に接続されている。本実施例1の半導体装置100の外周部131Sの電気的な接続は、導電性131Sの外周部131Sに設けられた半導体素子100からなる導電部131Aを介してプリント基板等へ接続されることにより行われる。同、実施例1の半導体装置において、必ずしも図1

180を返ける必要はなく、図1 (d) に示すような場合180を返けない状態の二つでも良い。

(10010) 実施例1の半導体装置100に使用のリードフレーム130は、42Xニッケル-鉄合金を主成分としたもので、そして、図9(a)に示すような形状をした。エッチングにより外形加工されたリードフレーム130Aを用いたものであり、端子柱部133部分や他の部分の厚さより両端に形成されたインナーリード部131をもつ、ダムバー136は厚さ防止する部のダムとなる。尚、図9(a)に示すような形状をした、エッチングにより外形加工されたリードフレーム130Aを、本実施例においては用いたが、インナーリード部131と端子柱部133以外に部分的に不要なものであるから、特にこの形状に限定はされない。インナーリード部131の厚さ1は40 $\mu$ m、インナーリード部131以外の厚さ1'は0.15mmでリードフレーム素材の厚さのままである。インナーリード部131以外の厚さは0.15mmに限らず更に薄い0.125mm、0.50mm程度でも良い。また、インナーリードピッチに0.12mmと近いピッチで、半導体装置の多素子化に対応できるものとしている。インナーリード部131の第2面131Aは平坦状でワイヤボンディングし易い形状となっており、図1(b)に示すように、第3面131Aと第4面131A'はインナーリード側へ凹んだ形状をしており、第2面131A'b(ワイヤボンディング面)を狭くしても他面的に強いものとしている。

(0011) 本実施例においては、インターリード13  
【の長さが短かく、インターリード13に3ミレが見  
えしうらい、図9(a)に示すような、インター  
リード先端がそれぞれ分離された形状のリードフレーム 30  
をニッチング加工して作製し、これに前述する方式に  
より半導体素子を取り付けて密封されている、インター  
リード13が長く、インターリード13に3ミレを見  
えしう場合場合には、図9(a)に示す形状にニッチ  
ング加工することは出来ないため、図9(c)(イ)に  
示すようにインターリード先端部を図9(b)にて  
固定した状態にニッチング加工した後、インターリード  
131部を図9(c)にて固定し、図9(c)に

(ロ) 次に、外でプレスにて、半導体実装作業の図には  
不揮の塗布膜！JIBを分離し、この状態で半導体素子  
を配置して半導体実装作業する。(図9(c))

(0012) 次に五等角例1の断面形状を、図9に示す。先ず、 $\frac{1}{8}$ 寸厚の鋼板を、図8に基づいて加工して成形する。先ず、 $\frac{1}{8}$ 寸厚の鋼板を、図8に基づいて加工して成形する。先ず、 $\frac{1}{8}$ 寸厚の鋼板を、図8に基づいて加工して成形する。

次に、 $\alpha$  成分は  $110^\circ$  の方位に  $111$  例の面を配して、 $\beta$  成分は分子をダイバッド  $135^\circ$  上に配し、図 50

とした。(8a (b)):

半導体電子110モダイバッド:35に選定したは  
は外電子110の製造員111とインターリード三  
1元増のヌ2座とをワイヤ:20にてハンデリンでさ  
した。(図8(c))

[illegible]

69に示すリードフレーム：30人のデータに12のフレーム及び7本を挿入した。この後、リードフレームの端子柱の外側の面に半導体の端子からなる半導体：30人を取り出して半導体基板を作製した。(59 (c))

ないで、重量は180を重量が190を介して両端子の  
側面を覆うように、外周全体に亘れた。(図8(1))  
向、重量は200は、半導体装置の減価のため、両端子  
の側面が露出することにより防止半導体と両端子の結合  
から水分が入り半導体装置にクラックが入り破壊してし  
まうことがないようにするみに設けたものであるが、必  
ずしも必要としない。また、重量による防止に所定の型  
を用いて行うが、半導体装置10のサイズで、且つ、  
「ドナー」の両端子の外側の面が若干重量から外縁  
へ突出した状態で防止した。

(0013) 本図の各部を裏面に用いられるリードフレームの製造方法を、図に示す。図1は、本図の「A」の部分に用いられるリードフレームの製造方法を説明するための、インターリ

こでは与えられるリードフレームを示す平面図である。図9 (a) のD1-D2線の新断面における公差工程である。E11E、1110はリードフレーム厚、1120A、1120Bはレジストパターン、1130にスーの開口、1140に第二の開口、1150に第一の凹部、1160に第二の凹部、1170に平坦表面、1180にニッチング抵抗面を示す。まず、42×ニッケル合金からなり、厚さが0.15mmのリードフレ

同とした本店に於てインレジストを並列した後、所定の  
パターンを用いて、所定形状の第一の導孔を110  
3-10に形成し、400℃で10分間加熱して、  
20A、1120Bを形成した。(図11(a))

第一の原稿第1130は、このエンチング加工においてリードフレーム2141110をこの開口部からベタ状にリードフレーム214より厚く形成せしめるためのもので、レジストの厚さの制御1140は、インターリード先端部のあはせを形成するためのものである。第一の原稿第1130は、少なくとも1つのリードフレーム11110のインターリード先端部を形成せしめるが、後工程において、

(10015) 向、上記図11、図12に示すエッチング加工方法のように、エッチングを2段階にわけて行うエッチング加工方法を、一般には2段エッチング加工方法といっており、本発明に開いた図9 (a) に示す、リードフレーム130Aの製造においては、2段エッチング加工で示す、パターンの形成を工完することにより部分的にリードフレーム基板を腐くしながらうね形成工をする方法とが採用して行われており、リードフレーム基板を腐くした部分においては、図11、図12に示す、上記の方法においては、インナーリード先図部1311Aの微細化加工は、上記の図91160の要部と、最終的に用いられるインナーリード先図部の厚さ1に左右されるもので、例えば、厚さ1を50μm

(0019)において、実施例2の取付防止型ニ導体基板を配ける。図4(a)は実施例2の取付防止型ニ導体基板の新断面図であり、図4(b)に図4(a)のA3-A4におけるインターリード部の新断面図で、図4(c)は図4(a)のB3-B4における電子柱部の新断面図である。尚、実施例2の半導体基板の外周は実施例1と同じと同じとなる。図は省略した。図中、「2」の数字は半導体基板、210には半導体素子、211には電極層(パッド)、220にはワイヤ、230はリードフレーム、231はインターリード、231Aは第1面、231Bは第2面、231Cは第3面、231Dは第4面、232は電子柱部、233Aは電子線、233Bは鉛面、233Cは上面、240は封止用樹脂、270は密封固定用テープある。実施例2のニ導体基板においては、リードフレーム230はダイバンドを持たないもので、半導体素子210はインターリード231ととともに密封固定用テープ270により固定されており、半導体素子210は、半導体素子の背面側(パッド)211



例にワイヤ230により、インナーリード231の第2面231Aとを接続されている。本実施例2の場合も、実施例1の場合と同様に、半導体装置200と外部回路との電気的な接続は、端子E233の元端子に接続された導体の半田からなる導体233Aを介してプリント基板へ施されることにより行われる。

(0020) また、本実施例2の半導体装置は、図10(a)、10(b)に示す、ダイバンドを用いた、ニッチングにより形成加工されたリードフレーム230Aを用いたもので、その製造方法には実施例1と同様であるが、また、本実施例1の場合には半導体素子をインナーリードに固定した状態でワイヤボンディングを行い、密着防止しているのに対し、本実施例2の場合には、半導体素子210をインナーリード231とともに密着固定用テープ270上に固定した状態で、ワイヤボンディング工程を行い、密着防止している点である。尚、密着防止後のプレスによる半導体部分の切断、端子部の形成は、実施例1と同様である。図10(a)に示すリードフレーム230Aを組むには、図9(a)に示すリードフレーム230Aを組む場合と同様に、図9(b)に示すリードフレーム230Aを組む場合と同様に、図9(c)に示すニッチング加工されたもののものを組み、図10(a)に示す状態にする。この際、図10(c)(c)に示すように、導体のため、導体テープ260(ポリイミドテープ)を使用する。

(0021) 図5(a)~図5(c)は、実施例2の半導体装置の実施例半導体装置の断面図である。図5

(a)に示す実施例半導体装置は、半導体素子の面を、図5(a)で、半導体素子を下側にしている点、およびワイヤボンディング面をリードフレームの第1面に

図5(b)、図5(c)に示す実施例半導体装置は、それぞれ実施例2の半導体装置、図5(a)に示す実施例の半導体装置において、半導体素子の半田からなる導体素子を、端子E233の側面233Bを介してプリント基板へ施されることにより行われる。

(0022) 次に、実施例3の密着防止型半導体装置を説明する。図6(a)は実施例3の密着防止型半導体装置の断面図であり、図6(b)は図6(a)のA5-A6におけるインナーリード部の断面図で、図6(c)は図6(a)のS5-B6における端子E333の断面図である。尚、実施例3の半導体装置の外観は実施例1と同様となる。図に示した、図6中、300は半導体装置、310は半導体素子、312はパッド、330はリードフレーム、331はインナーリード、331Aは第1面、331ABは第2面、331Aと331Bは第3面、331Aと331Bは第4面、333は端子E333、333Aは端子E333Bは側面、333Sは上面、340は

半導体装置、350は密着固定用テープである。本実施例3の半導体装置においては、半導体素子310は、パッド311によりインナーリード331の第2面331ABとに固定され、電気的にインナーリード331と接続している。リードフレーム330は、図10(a)、図10(b)に示す形状のもので、図11に示すニッチング加工により形成加工されたものを用いている。図11(a)(b)に示すように、インナーリード331の第2面331AB、W2A(約100μm)ともこの部分の幅350

10 方向の幅W2Aよりも大きくなっており、且つ、インナーリード331の第2面331ABはインナーリードの内部に向かって凹んだ形状で、第1面331Aが凹みであることより、インナーリードの固定化に対応できるとともに、インナーリード331の第2面331Aとにおいて、半導体素子とパッドにて電気的に接続する口には、図13(c)(b)のように接続がし易いものとしている。また、本実施例3の場合も、実施例1や実施例2の場合と同様に、半導体装置200と外部回路との電気的な接続は、端子E333の元端子に接続された導体の半田からなる導体233Aを介してプリント基板へ施されることにより行われる。

(0023) 実施例3の半導体装置は、実施例1の半導体装置の場合と同様に、図12に示すニッチングにより形成加工されたリードフレームを用いたものである。

また、本実施例3の半導体装置の場合には半導体素子をインナーリードに固定した状態でワイヤボンディングを行い、密着防止しているのに対し、本実施例3の半導体装置の場合には、半導体素子310をインナーリード331にパッドを介して固定して電気的に接続した状態で密着防止している点である。尚、密着防止後のプレスによる半導体部分の切断、端子部の形成は、実施例1の半導体装置の場合と同様である。

(0024) 図6(a)は、実施例3の半導体装置の実施例半導体装置の断面図である。図6(b)に示す実施例半導体装置は、実施例3の半導体装置において、半導体素子の半田からなる導体素子を、端子E333の側面233Bを介してプリント基板へ施されることにより行われる。図6(c)は図6(a)のA7-A8におけるインナーリード部の断面図で、図6(c)は図6(a)のS7-B8における端子E333の断面図である。尚、実施例4の半導体装置の外観は実施例1と同様となる。図に示した、図7中、400は半導体装置、410は半導体素子、411はパッド、430は

(0025) 次に、実施例4の密着防止型半導体装置を説明する。図7(a)は実施例4の密着防止型半導体装置の断面図であり、図7(b)は図7(a)のA7-A8におけるインナーリード部の断面図で、図6(c)は図6(a)のS7-B8における端子E333の断面図である。尚、実施例4の半導体装置の外観は実施例1と同様となる。図に示した、図7中、400は半導体装置、410は半導体素子、411はパッド、430は

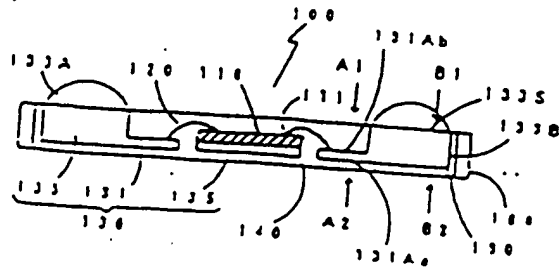
リードフレーム、431はインターリード、431Aa  
に第1面、431Abは第2面、431Acは第3面、  
431Adは第4面、433は第5面、433Aは第  
6面、433Bは第7面、433Cは第8面、440は封  
止層材、470は絶縁性層材である。本実施例の場  
合は、半導体素子410のパッド311側の面をインテ  
ーリード331の第2面431Abに絶縁性層材47  
0を介して固定し、パッド411とインターリード43  
1の第1面431Aaとをワイヤ420にて電気的に固  
定したものである。使用するリードフレームは実施例3  
と同一、図10(a)、図10(b)に示す形状の  
ものを使用している。また、本実施例4の場合も、実  
施例1や実施例2の場合と同様に、半導体素子400と  
外部回路との電気的な接続は、素子座333先端部に設  
けられた半導体素子の半田からなる端子部433Aを介して  
プリント基板等へ接続されることにより行われる。  
(0026) 図7(c)は、実施例4の半導体素子の文  
形例半導体素子の断面図である。図7(c)に示す実  
例半導体素子は、実施例4の半導体素子において、半  
導体の半田からなる端子部を設けず、端子座の底面を  
端子部として用いているものである。底面材を無くして  
端子座433の側面433Bを側面に露出している。テ  
スタ等での接点のテニクがし易い構造となっている。  
(0027)  
(発明の効果) 本発明の回路封止型半導体装置は、上記  
のように、リードフレームを用いた回路封止型半導体  
装置において、多層化に対応でき、且つ、従来の図13  
(b)に示すアフターリードを持つリードフレームを用  
いた場合のようにダムバーのカット工程や、ダムバーの  
設け工程を必要としない。即ち、アフターリードのスネ  
ューの問題や、半導体座にコープラナリチエーの形成工  
程を省くことができる半導体装置の提供を可能としている。ま  
た、QFPやBGAに比べるとパッケージ内部の配線長  
が短くなるため、寄生容量が小さくなり高速動作を  
可能にしている。  
(図面の簡単な説明)  
(図1) 実施例1の回路封止型半導体装置の断面図  
(図2) 実施例1の回路封止型半導体装置の斜視図  
(図3) 実施例1の回路封止型半導体装置の外形図  
(図4) 実施例2の回路封止型半導体装置の断面図  
(図5) 実施例2の回路封止型半導体装置の外形図  
(図6) 実施例3の回路封止型半導体装置の断面図  
(図7) 実施例4の回路封止型半導体装置の断面図  
(図8) 実施例1の回路封止型半導体装置の接点部を  
説明するための図  
(図9) 本発明の回路封止型半導体装置に用いられるリ  
ードフレームの図  
(図10) 本発明の回路封止型半導体装置に用いられる  
リードフレームの図

(図11) 本発明の回路封止型半導体装置に用いられ  
るリードフレームの作製方法を説明するための図  
(図12) 本発明の回路封止型半導体装置に用いられ  
るリードフレームの作製方法を説明するための図  
(図13) インターリード先端部でのワイヤボンディング  
の断面図を示す図  
(図14) 従来のリードフレームのニッテング工程を  
説明するための図  
(図15) 本発明の回路封止型半導体装置及び回路リ  
ードフレームの図  
(符号の説明)  
100、200、300、400  
回路封止型半導体装置  
110、210、310、410  
半導体素子  
111、211、411  
底 (パッド)  
312  
チップ  
120、220、420  
ワイヤ  
120A、120B  
ワイヤ  
121A、121B  
ワイヤ  
130、230、330、430  
リードフレーム  
131、231、331、431  
インターリード  
131Aa、231Aa、331Aa、431Aa 第  
1面  
131Ab、231Ab、331Ab、431Ab 第  
2面  
131Ac、231Ac、331Ac、431Ac 第  
3面  
131Ad、231Ad、331Ad、431Ad 第  
4面  
131B  
第5面  
133、233、333、433  
端子部  
133A、233A、333A、433A  
端子部  
133B、233B、333B、433B  
第6面  
133C、233C、333C、433C  
第7面  
140、240、340、440  
絶縁層材  
150

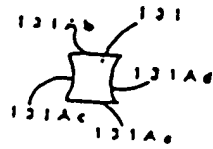
190		ードフレーム部材	
260	材	1331A b	
270		イニング部	ニ
270	材	1410	
270	材	ードフレーム部材	リ
350	材	1420	
470	材	オートレジスト	フ
1110	材	1430	
1120A, 1120B	材	ジストパターン	レ
1130	材	1440	
1140	材	ンナーリード	イ
1150	材	1510	
1160	材	ードフレーム	リ
1170	材	1511	
1180	材	イパッド	グ
1190	材	1512	
1200	材	ンナーリード	イ
1210	材	1512A	
1220	材	ンナーリード先端部	フ
1230	材	1513	
1240	材	クターリード	フ
1250	材	1514	
1260	材	ムバー	グ
1270	材	1515	
1280	材	レーム部 (材部)	フ
1290	材	1520	
1300	材	部材表示	半
1310	材	1521	
1320	材	部材 (パッド)	電
1330	材	1530	
1340	材	1540	
1350	材	止用部材	フ
1360	材		
1370	材		
1380	材		
1390	材		
1400	材		
1410	材		
1420	材		
1430	材		
1440	材		
1450	材		
1460	材		
1470	材		
1480	材		
1490	材		
1500	材		
1510	材		
1520	材		
1530	材		
1540	材		
1550	材		
1560	材		
1570	材		
1580	材		
1590	材		
1600	材		
1610	材		
1620	材		
1630	材		
1640	材		
1650	材		
1660	材		
1670	材		
1680	材		
1690	材		
1700	材		
1710	材		
1720	材		
1730	材		
1740	材		
1750	材		
1760	材		
1770	材		
1780	材		
1790	材		
1800	材		
1810	材		
1820	材		
1830	材		
1840	材		
1850	材		
1860	材		
1870	材		
1880	材		
1890	材		
1900	材		
1910	材		
1920	材		
1930	材		
1940	材		
1950	材		
1960	材		
1970	材		
1980	材		
1990	材		
2000	材		

( 1 )

(a)



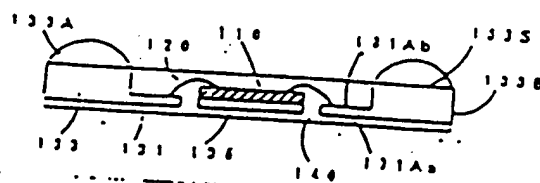
(b)



(c)

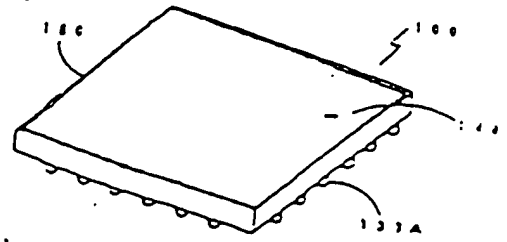


(d)



( 2 )

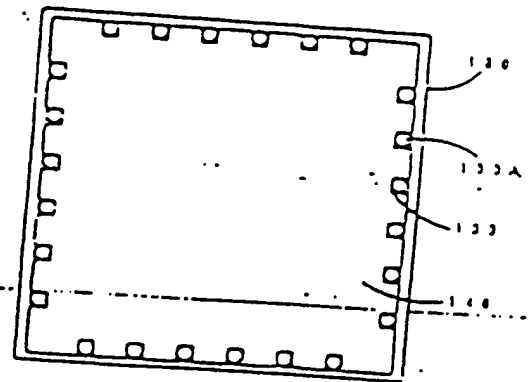
(a)



(b)

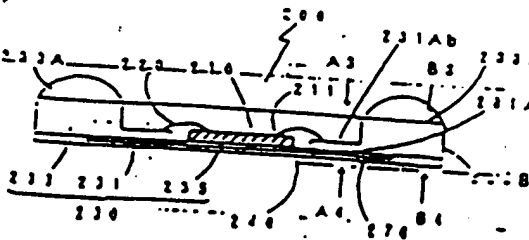


(c)

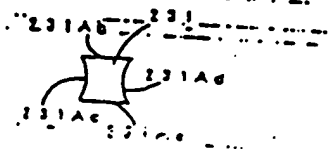


( 4 )

(a)



(b)

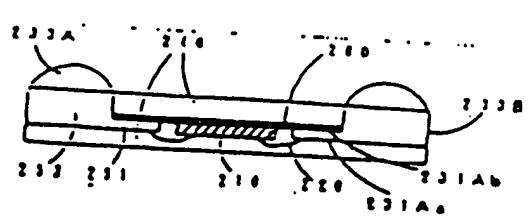


(c)

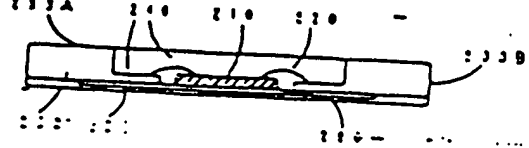


( 5 )

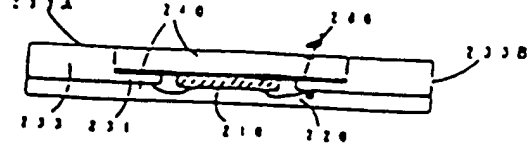
(a)



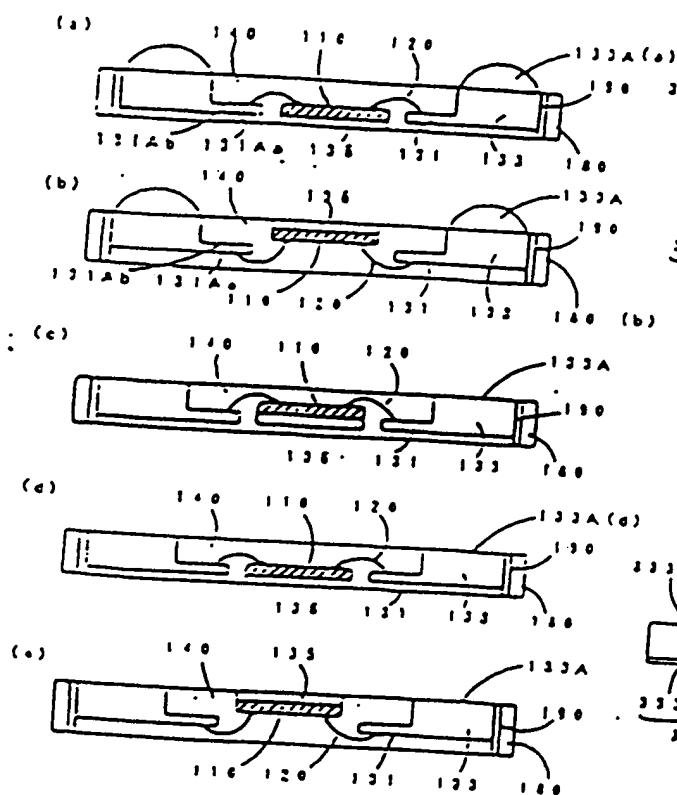
(b)



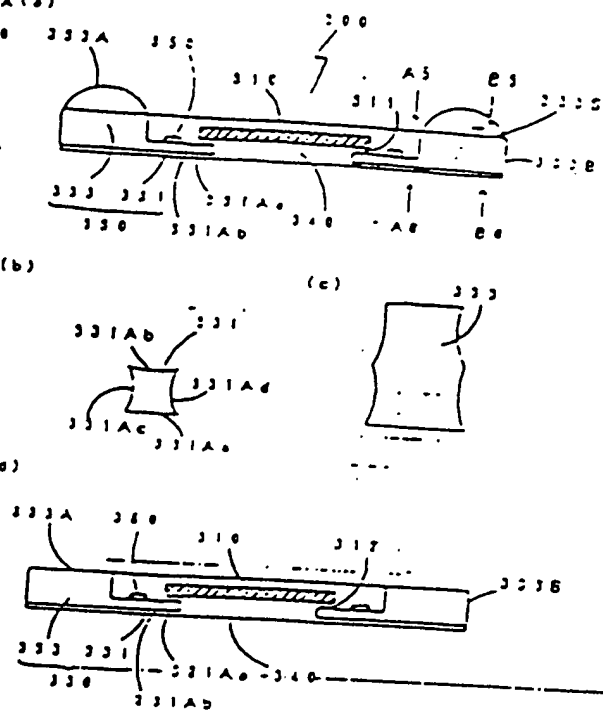
(c)



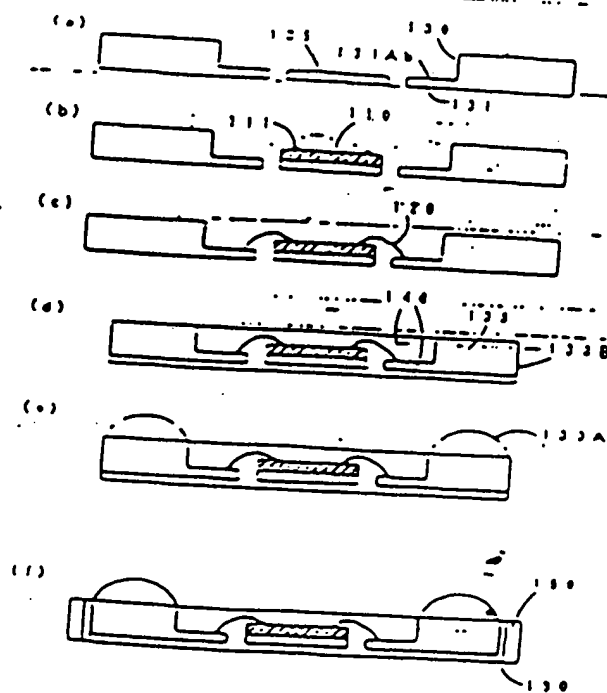
( ५३ )



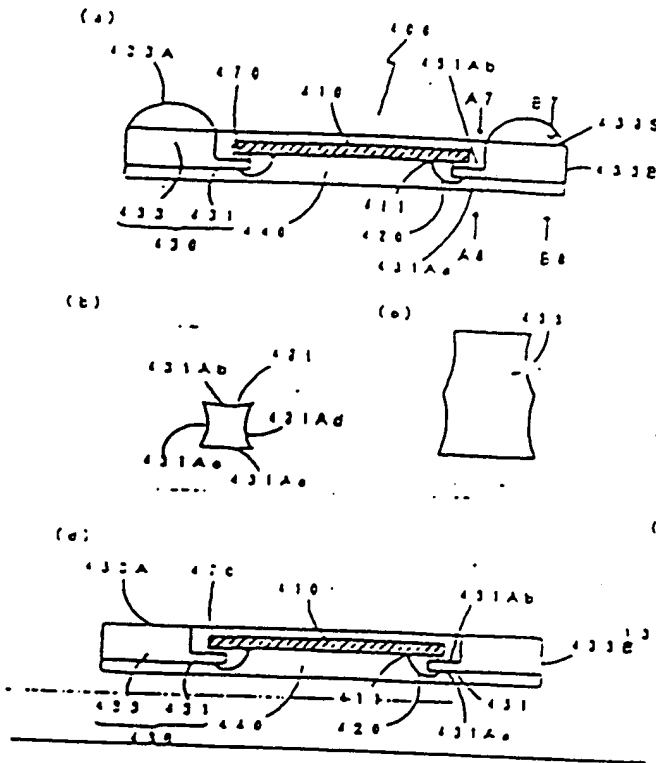
( 56 )



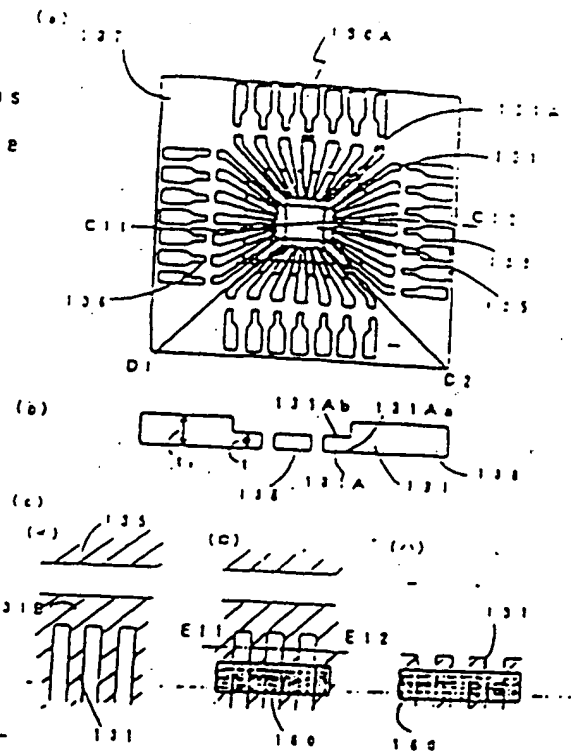
( 9 2 )



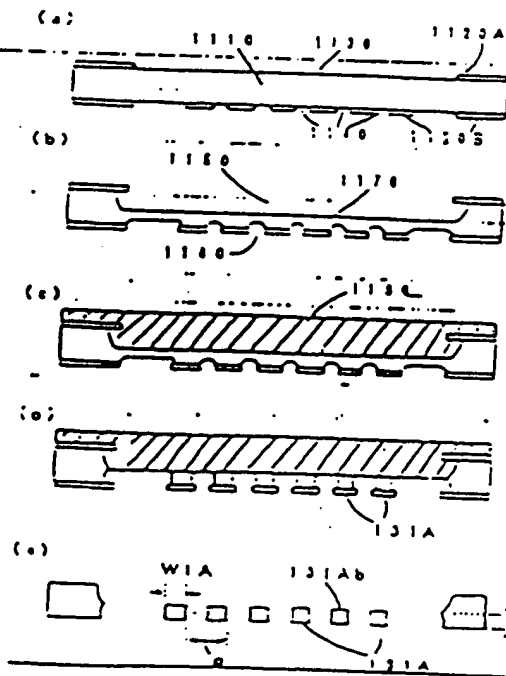
( 27 )



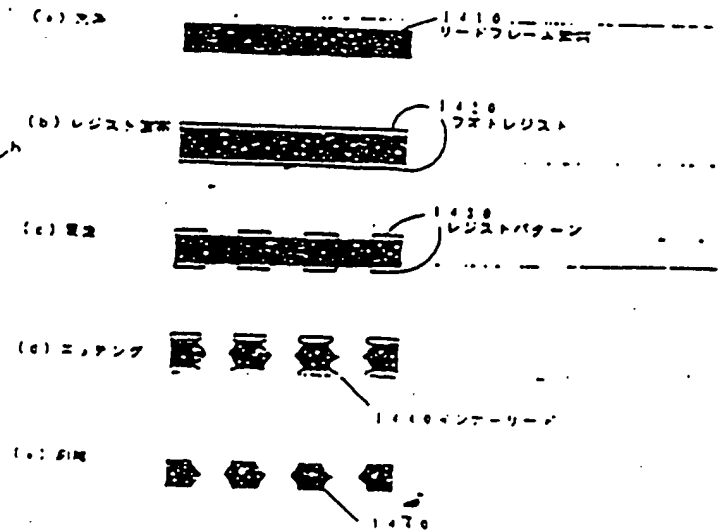
( 29 )



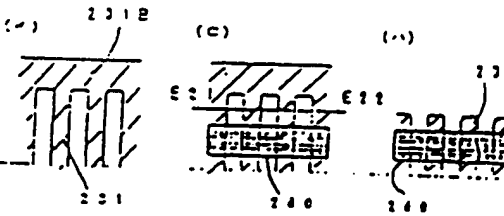
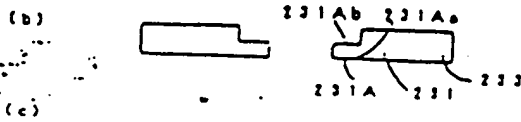
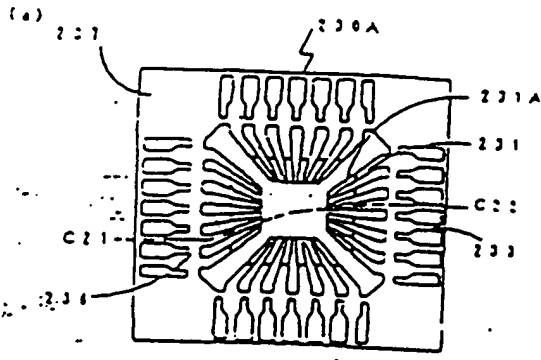
( 31 )



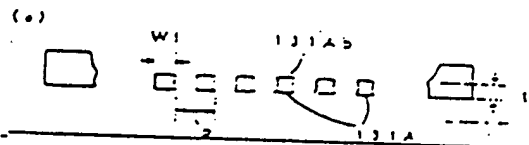
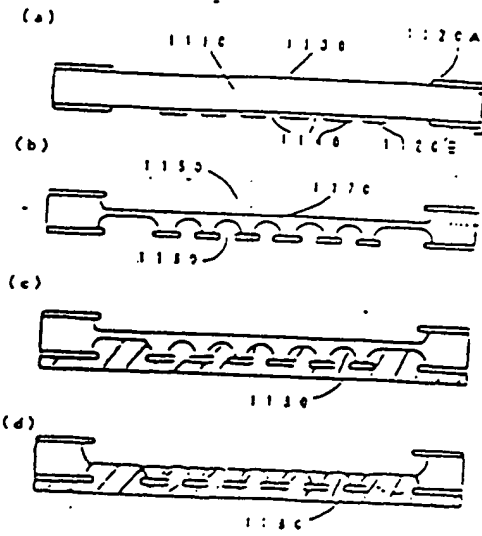
( 34 )



(210)



(212)



(215)

